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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,397	04/20/2007	Xiaokun Xiong	20016.0001USWO	2501
52835 7590 09/08/2010 HAMRE, SCHUMANN, MUELLER & LARSON, P.C. P.O. BOX 2902 MINNEAPOLIS, MN 55402-0902				
EXAMINER				
MISIURA, BRIAN THOMAS				
ART UNIT		PAPER NUMBER		
2111				
MAIL DATE		DELIVERY MODE		
09/08/2010		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/583,397

Applicant(s)

XIONG, XIAOKUN

Examiner

BRIAN T. MISIURA

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☒ Claim(s) 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 June 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SG-08)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date 8/31/2006

Detailed Action

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 8/31/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to because they comprise a typographical error: Figure 7 numeral 706 cites "write *bugger*" as opposed to "write *buffer*".

3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because Page 11 line 21 comprises a typographical error. The Examiner believes that "dynamatically" should read "dynamically". Appropriate correction is required.

Claim Objections

5. Claim 13 is objected to because of the following informalities: "dynamatically" should read "dynamically", "between" should read "between", and "bus request signal" should read "bus interface multiplexing request signal" as introduced in claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. The term "i960-like" is a relative term which renders the claim indefinite. The term "i960-like" is not definite by the claim, the specification does not provide a standard for ascertaining the requisite degree to which a bus protocol qualifies as "i960-like", and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

8. Claim 1 recites the limitations "the address bus" and "the data bus". There is insufficient antecedent basis for these limitations in the claim.

9. Claim 6 recites the limitation "the request and response function" and "accessing outside shared bus". There is insufficient antecedent basis for these limitations in the claim.

10. Claim 6 is indefinite because the limitations which comprise insufficient antecedent basis make the interpretation of the claim as a whole unclear. For examination purposes, the claim will be given the interpretation of using a multiplexing technique to connect two busses.

11. Claim 8 recites the limitations "bus request signal", "the state indicating signal", and "response signal". There is insufficient antecedent basis for these limitations in the claim.

12. Claim 8 is indefinite because the limitations which comprise insufficient antecedent basis make the interpretation of the claim as a whole unclear. For examination purposes, the claim will be given the interpretation of multiplexing a bus request.

13. Claim 9 recites the limitations "the address and data multiplexing output bus", "the top interconnected logic module", "ADS-IN", and "tri-state gate". There is insufficient antecedent basis for these limitations in the claim.

14. Claim 9 is indefinite because the limitations which comprise insufficient antecedent basis make the interpretation of the claim as a whole unclear. For examination purposes, the claim will be given the interpretation of a multi-state multiplexer.

15. Claim 10 recites the limitations "AHB bus clock" and "i960-like bus clock". There is insufficient antecedent basis for these limitations in the claim.

16. Claim 11 recites the limitation "the clock frequency". There is insufficient antecedent basis for this limitation in the claim.

17. Claim 13 recites the limitations "the clock of the i960-like interface", "the i960-like interface clock", and "the bus clock of the i960-like interface". There is insufficient antecedent basis for these limitations in the claim. If the cited limitations are meant to refer to the same "clock", they should be amended to be consistent with each other.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. Claims 1 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. U.S. Patent No. 6,996,659 in view of Ezzet, U.S. Patent No. 5,603,051.

19. Per claim 1, Lupien Jr. discloses: a bus interface converter capable of converting AMBA AHB bus protocol into i960-like bus protocol (**Column 2 lines 22-39 and Figure 1 discloses that the busses may comprise embedded processor busses. An embedded processor bus is considered one of the broadly claimed "i960-like" bus protocols. Column 14 last paragraph and Figure 10 disclose an AHB bus. For the remainder of the reference citations, Bus 1 of Lupien will refer to the AHB bus and Bus 2 of Lupien will refer to an "i960-like" bus.**), wherein the converter

comprising: an AHB interface for accomplishing interface processing for AMBA AHB bus protocol (**Figure 1; Bus 1 specific logic 106**); an i960-like interface for accomplishing interface processing for i960-like bus protocol (**Figure 1; Bus 2 specific logic 108**); and a main controller for accomplishing bus protocol conversion between the AHB interface and the i960-like interface (**Figure 1, Bridge 100 comprises routing manager 162. Column 12 last paragraph, Figure 9.**); wherein, the AHB interface comprising: an AHB bus signal register module for accomplishing judgment and register for control signal from an AMBA AHB bus (**Column 3 lines 15-33, Figure 2; Bus 1 master sequencer 116a**); and an AHB bus signal response module for generating corresponding response indicating signal of AMBA AHB bus protocol (**Column 4 lines 25-37, Figure 2; Bus slave sequencer 116b**); the i960-like interface comprising: a bus interface multiplexing request module for generating bus interface multiplexing request signal (**Column 4 lines 6-24 and last paragraph, Figure 2; Bus 2 master sequencer 126a**); and a bus multiplexing module for accomplishing the multiplexing between the address bus for outputting from AHB to i960-like and the data bus for outputting from AHB to i960-like (**Column 9 line 59 – Column 10 line 6; Figure 4 numeral 170b**).

Lupien Jr. discloses a generic bridge for coupling two or more busses; and wherein the busses may comprise embedded processor busses. The disclosure of Lupien Jr. is presented with the first bus being an AHB bus and the second bus being a PCI-X bus (Figure 10). Lupien Jr. does not specifically mention "i960" in the disclosure but it is well known in the art that i960 refers to a RISC-based processor from Intel and thus an embedded processor bus may vary well be an "i960" bus.

However, for full disclosure, Ezzet is provided to teach that it is well known in the art for an i960 bus protocol to be coupled to a second bus protocol via a bridging circuit (**Column 6 last paragraph, Figure 5**).

- It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an i960 protocol bus as taught by Ezzet as the second bus

of Lupien Jr. because it qualifies as an embedded processor bus. Additionally, both Lupien Jr. and Ezzet are from the same field of endeavor (different protocol bus bridging).

20. Per claim 6, Lupien Jr. discloses multiplexer 170 for multiplexing two busses **(Column 12 first paragraph, Figure 4. See also 112 second paragraph rejection above.)**.

21. Per claim 7, Lupien Jr. discloses the converter according to claim 1, wherein the i960-like interface can be directly connected to i960-like bus **(Figure 1 numerals 108 and 104)**.

22. Per claim 8, Lupien Jr. discloses wherein the bus interface multiplexing request module determines whether to send bus request signal to the bus interface unit based on the state indicating signal from the main controller, and determines whether to stop sending bus request signal to the bus interface multiplexing controller based on response signal from i960-like bus **(Column 4 lines 6-24 and last paragraph, Figure 2; Bus 2 master sequencer 126a. See also 112 second paragraph rejection above.)**.

23. Per Claim 9, Lupien Jr. discloses a multiplexing module **(Column 9 line 59 – Column 10 line 6; Figure 4 numeral 170b. See also 112 second paragraph rejection above. Additionally, Abdelnour et al. U.S. PN 6,112,241 disclose multiplexer units 26 that select from up to N inputs, Figure 4 and tri-state circuitry 35 connected to an i960 processor bus, Figure 2.)**

24. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. U.S. Patent No. 6,996,659 in view of Ezzet, U.S. Patent No. 5,603,051 in further view of Jahnke et al. U.S. Patent No. 6,829,669.

25. Per claim 2, Lupien Jr. discloses data buffers 166, but does not specifically disclose the limitations of claim 2.

However, Jahnke discloses an AHB to HTB (high performance data transfer bus) bus bridge 315 that includes a write buffer (**FIFO's 510 and 520**) for latching the full address and data from the AHB bus 300 (**Column 4 last paragraph, Figures 3 and 5**).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to implement the data/address write buffers of Jahnke within the buffering scheme of Lupien Jr. because the AHB bus comprises both address and data busses and both the address and data information are necessary for completing the transaction.

26. Per claim 3, Jahnke further discloses wherein the AHB bus write buffer module comprises two buffering fields: address field and data field (**Column 4 last paragraph; Address FIFO 510 and Data FIFO 520**). Please refer to claim 2 for motivation to combine the references.

27. Per claim 4, Jahnke further discloses wherein the AHB bus write buffer module has an enabling port, and can set the size of buffering fields for the address field and data field of the AHB bus write buffer module via AHB bus (**Column 6 lines table 1**). Please refer to claim 2 for motivation to combine the references.

28. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. U.S. Patent No. 6,996,659 in view of Ezzet, U.S. Patent No. 5,603,051 in further view of Stewart, U.S. Patent No. 6,789,153.

29. Per claim 5, Lupien Jr. does not specifically disclose the HREADYout and HRESP signals.

However, Stewart discloses a plurality of signals that pass through AHB bus bridge 20, including HREADYout and HRESP signals (**Table 1**).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention for the AHB specification signals as disclosed by Stewart to be utilized within the AHB system of Lupien Jr. since the signals are inherent to the protocols specification.

30. Per claim 12, Lupien Jr. does not specifically disclose a state machine.

However, Stewart discloses AHB bus bridge 20 comprising a state machine 51 where the state machine controls the overall function of the bridge (**Column 5 lines 10-16**). Stewart further discloses that the state machine includes the three states of idle, read, and write (**Figure 7**).

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention for the bridging circuitry of Lupien Jr. to include a state machine like that of Stewart because it controls the overall function of a bridging circuit by performing functions as they were designed in an attempt to avoid error conditions.

31. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lupien Jr. et al. U.S. Patent No. 6,996,659 in view of Ezzet, U.S. Patent No. 5,603,051 in further view of Fuks U.S. Patent No. 7,165,184.

32. Per Claim 10, Lupien Jr. does not specifically disclose wherein the main

controller has two clocks being synchronous with AHB bus clock and i960-like bus clock respectively.

However, Fuks discloses bridging two different bus protocols via a bridge 30, where the each of the busses clock domains are utilized in latching data from the respective buses **(Column 2 lines 6-23)**.

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to implement the bus clock domain functionality of the bridge of Fuks within the bridging circuit of Lupien Jr. because it is less expensive to implement than independent clock schemes which require additional remapping circuitry.

33. Per Claim 11, Lupien Jr. does not specifically disclose the relationship of the clock frequencies of the two busses being bridged.

However, Fuks discloses wherein the clock frequency of a first bus may be N times of that of the a second bus, where N is a natural number no less than 1 **(Column 3 lines 32-54; AHB bus 20 may be 78 MHz which is 6 times greater than the LPFAB bus 28 at 13 MHz)**.

- It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention for a first bus to have a frequency N times greater than a second bus it is being bridged to because systems comprises a plurality of busses of varying frequencies based upon what their intended functioning is.

Allowable Subject Matter

34. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the

base claim; and rewritten to overcome the numerous outstanding claim objections and 112 second paragraph rejections of the base claim and claim 13.

35. The following is a statement of reasons for the indication of allowable subject matter:

36. Claim 13 is considered to be containing allowable subject matter, primarily due to the bus interface multiplexing request signal acting as a control signal for the i960-like bus clock output while operating in a low power mode; in combination with the other existing limitations of claim 1 and claim 13.

37. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art

38. The prior art made of record but not relied upon in the Examiner's rejections is provided below along with the reasoning for considering it pertinent to the applicant's disclosure.

39. U.S. Patent No.'s 6,442,642 and 6,571,308 disclose Advanced High-Performance Bus (AHB) bridging techniques.

40. U.S. Patent No.'s 6,161,161; 6,122,670; 6,112,241; and 6,065,087 all disclose i960 protocol bridging techniques.

41. The Non-Patent Literature (NPL) documents cited are considered pertinent because they at least one of the pertinent topics: i960/80960 processor architecture and AMBA specification.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Brian T Misiura/

Patent Examiner, Art Unit 2111